REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In the present Office Action, Claims 1-3, 5-14 and 16-20 stand rejected under 35 U.S.C. §103 as allegedly unpatentable over the combined disclosures of U.S. Patent No. 5,298,845 to Verret ("Verret") and U.S. Patent No. 6,207,534 to Chan, et al. ("Chan, et al."). Claims 4 and 15 stand rejected under 35 U.S.C. §103 as allegedly unpatentable over the combined disclosures of Verret, Chan, et al. and U.S. Patent No. 6,150,212 to Divakaruni, et al. ("Divakaruni, et al.").

Applicants respectfully submit that the combined disclosures of Verret and Chan, et al., or Verret, Chan, et al. and Divakaruni, et al. do not render applicants' claimed methods obvious since none of the applied references teaches or suggests a method which includes, among other steps: *forming a plurality of apertures (or first trench isolation regions) having a first depth in an unblocked region of a semiconductor substrate using a patterned masking layer to define the plurality of first trench isolation regions by first removing exposed portions of a pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate; and forming a plurality of second aperture (or trench isolation regions) having a second depth in regions of said semiconductor substrate that were previously blocked by a first block mask using said patterned masking layer to define said second trench isolation regions, while simultaneously increasing said first depth such that said first depth is deeper than said second depth, said second trench isolation regions are formed by first removing said exposed portions of said pad stack to expose portions of*

said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate.

Thus, in the claimed methods, the first and second apertures (and first and second trenches) have sidewalls that are aligned to outer edges of the top patterned masking layer. In the claimed invention, the top patterned masking layer is employed as a single critical mask that is used in defining each of the apertures.

Verret discloses a method which includes the steps of depositing a SiN layer 34 and a first photoresist layer on a surface of substrate 30 which includes SiO_2 layer 32 formed thereon; patterning the first photoresist layer to provide patterned photoresist 36 which has openings that expose SiN layer 34; etching the exposed SiN layer and removing the first photoresist layer; forming second photoresist layer 42 having opening 44 on the now patterned SiN layer; etching a first trench 46 into the substrate through opening 42; removing the second photoresist layer; and etching to provide second trench 52 while deepening the first trench.

Thus, in Verret, a first masking layer 36 is required to pattern SiN layer 34, and neither the first masking layer 36 nor the patterned SiN layer 34 is used to define the first trench or aperture. Instead, a second patterned photoresist 42 is used in defining the first trench. As a consequence, the first trench has sidewalls that are aligned with the second photoresist, not the patterned SiN layer 34. In Verret, the second photoresist is used as the critical mask in defining the first trench.

Applicants respectfully submit that in Verret, the second trench as well as the upper portion of the first trench have sidewalls that are aligned to the patterned SiN

layer 34; the lower portion of the first trench disclosed in Verret does not have sidewalls aligned to the patterned masking layer 34.

Applicants thus submit that in Verret two different critical masks; second photoresist 42 and patterned SiN layer 34, are used in defining the trenches.

In the claimed methods, however, the first and second apertures (or first and second trench isolation regions) are formed using the same critical mask. As a consequence, the sidewalls of the first and second apertures (or first and second trench isolation regions) have sidewalls that are aligned with the outer edges of the top patterned masking layer.

Chan, et al. do not alleviate the above defects in Verret since the applied secondary reference also does not teach or suggest applicants' claimed methods which include the processing steps recited in the claims of the present invention. Chan, et al. provide a method of forming trenches having different depths. In accordance with the process disclosed in Chan, et al., the different trench depths are formed by depositing an oxide layer overlying a silicon substrate; etching through the oxide layer to the top surface of the silicon substrate to form openings for planned first trenches; depositing a polysilicon layer overlying the oxide layer and filling the openings for the planned first trenches; polishing down the polysilicon layer to the top surface of the oxide layer such that the polysilicon layer remains only in the openings of the planned first trenches; thereafter etching through the oxide layer to the top surface of the silicon substrate to form openings for planned second trenches; *etching simultaneously the silicon substrate and the polysilicon to complete the first trenches and the second trenches, wherein said*

etching forms second trenches deeper than first trenches; and completing the fabrication of the integrated circuit device.

In accordance with the process disclosed in Chan, et al., different trench depths are formed into the Si substrate during a single etching step, See FIG. 9. This is achieved in the prior art by providing a placeholder material of polysilicon 42 in a predetermined position on the surface in which the first trenches are to be formed, while exposing other areas of the substrate in which second trenches are to be formed. During the etching step, the polysilicon and Si substrate, which are both exposed, are simultaneously etched using chemistry that selectively removes silicon. The depth of the trenches is controlled by absence or presence of the polysilcon layer 42. See. Col. 4, lines 15-16.

This is different from the claimed invention in which *a plurality of apertures (or first trench* isolation *regions) having a first depth in an unblocked region of a semiconductor substrate is first formed using a patterned masking layer to define the plurality of first trench isolation regions by first removing exposed portions of a pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate; and thereafter forming a plurality of second aperture (or trench isolation regions) having a second depth in regions of said semiconductor substrate that were previously blocked by a first block mask using said patterned masking layer to define said second trench isolation regions, while simultaneously increasing said first depth such that said first depth is deeper than said second depth, said second trench isolation regions are formed by first removing said*

exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate.

Applicants respectfully submit that the combination of Verret and Chan, et al. would utilize a method of forming different depth trenches using the technique disclosed in Chan, et al.

The other applied reference cited in the present Office Action, i.e., Divakaruni, et al., is further removed from the claimed method than either Verret or Chan, et al. as evident by the fact that the Examiner has relied on Divakaruni, et al. for disclosing the types of patterned masking layers defined in dependent Claims 4 and 15. Applicants find no disclosure in Divakaruni, et al. that teaches or suggests using the patterned masking layer to define a first trench, and thereafter a second trench, wherein the first trench is deeper than the second trench. As such, the combination of Verret, Chan, et al. and Divakaruni, et al. does not render applicants' claimed method obvious.

The §103 rejections also fail because there is no motivation in the applied references which suggests modifying the methods disclosed therein to include applicants' claimed processing steps. This rejection is thus improper since the prior art does not suggest this drastic modification. The law requires that a prior art reference provide some teaching, suggestion, or motivation to make the modification obvious.

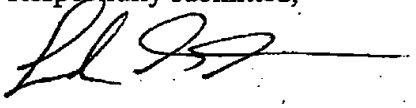
Here, there is no motivation provided in the disclosures of the applied prior art references, or otherwise of record, which would lead one skilled in the art to modify the methods of the applied references to include applicants' claimed sequence of processing steps recited in Claims 1 and 12 that lead to the formation of apertures or trenches of different depths. "The mere fact that the prior art may be modified in the

manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d, 1260,1266, 23 USPQ 1780,1783-84 (Fed. Cir. 1992).

Based on the above amendments and remarks, the §103 rejections have been obviated; therefore reconsideration and withdrawal of the instant rejections are respectfully requested.

Wherefore reconsideration and allowance of the claims of the present application are respectfully requested.

Respectfully submitted,



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